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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
SEMENENKO, YURIY	
ART UNIT	**PAPER NUMBER**
2841	

DATE MAILED: 10/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/650,395	SINGH, PRASHANT K.	
	Examiner	Art Unit	
	Yuriy Semenenko	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-20 is/are pending in the application.

4a) Of the above claim(s) 7-18 is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-6,19 and 20 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 28 August 2005 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. 1. Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1-6 and 19-20 drawn to an integrated circuit, classified in class 361 subclass 640.

II. Claims 7-18 drawn to an apparatus, classified in class 257 subclass 531.

1.2. The inventions are distinct, each from the other because of the following reasons: Inventions II and I are related as combination and subcombination. Inventions in this relationship are distinct if it can be shown that (1) the combination as claimed does not require the particulars of the subcombination as claimed for patentability, and (2) that the subcombination has utility by itself or in other combinations (MPEP § 806.05(c)). In the instant case, the combination as claimed does not require the particulars of the subcombination as claimed because an apparatus as claimed can be done with different type of transistors (without gallium arsenide pseudomorphic high-electron mobility transistors). The subcombination has separate utility such as an integrated circuit can work for devices when a value of said negative capacitance is not equal in magnitude to said capacitance associated with metal layers adjacent to said inductor layer.

1.3. Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, and the search required for Group II is not required for Group I, restriction for examination purposes as indicated is proper.

1.4. During a telephone conversation with C. W. Swantz (Registration No. 46329), on August 22, 2005, a provisional election without traverse was made to prosecute the invention of Group I, claims 1-6 and 19-20, drawn to an integrated circuit. Affirmation of this election must be made by applicant in replying to this Office action. Claims 7-18 drawn to an apparatus withdrawn from

further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

Claim Objections

2. Claim 14 objected to because of the following informalities:
In contest of claim 14 "An integrated circuit" should be changed to – An apparatus— because limitations of the claim 14 includes limitation "housing" and all apparatus claims 15-18 depends on claim 14.
Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3.1. Claims 1-6, 19 and 20 are rejected under 35U.S.C. 103(a) as being obvious over Forbes (Patent #6201287 hereinafter "Forbes") in view of Gagne et al. (Patent #6385019 hereinafter "Gagne") and in further view of Grzegorek (Patent # 5760456) hereinafter "Grzegorek").

3.1.1. Regarding claims 1and 19: Forber discloses in Fig. 9 an integrated circuit, comprising: a substrate 100; a plurality of metal layers (column 5, lines 1-8); an inductor layer 32 disposed within said plurality of metal layers; and a circuitry for generating a negative impedance (column 6, lines 52-58), said circuitry generating said negative impedance of a value to compensate for a impedance (column 5, lines 1-3), said circuitry being coupled to said inductor layer.

However, Forber doesn't teach a negative impedance is a negative capacitance and said circuitry generating said negative capacitance of a value to compensate for a capacitance associated with metal layers adjacent to said inductor layer.

Gagne discloses in the "Background of the invention" section, at the time the invention was made, it was well know to use a circuitry for generating a negative capacitance, said circuitry generating said negative capacitance of a value to compensate for a capacitance associated with metal layers adjacent to said inductor layer (column 2, lines 4-6). And further examiner notes, Forber's the prior art structure is capable of performing the intended use also.

Therefore it would have been obvious to one of ordinary skill in the art, at time the invention was made for Forber to include in his invention a negative impedance is a negative capacitance and said circuitry generating said negative capacitance of a value to compensate for a capacitance associated with metal layers adjacent to said inductor layer, as taught by Gagne because Gagne teaches that capacitances can be compensated provided a negative capacitance is generated as input impedance of the associated compensating circuit (column 2, lines 4-6).

Forber, however, fails also to expressly disclose a first metal layer being disposed on said substrate.

Grzegorek discloses in Fig. 3 an integrated circuit, comprising: a substrate 20; a first metal layer (ground layer at least) 22 and 32 being disposed on said substrate 20. Therefore, at time the invention was made, it was well know to use metal layer being disposed on said substrate.

Therefore it would have been obvious to one of ordinary skill in the art, at time the invention was made, for Forber to include in his invention that a first metal layer of said plurality of metal layers being disposed on said substrate, motivated by its known suitability for its intended use. See MPEP §2144.07.

3.1.2. Regarding claims 2 and 20: Forber discloses in Fig. 9 the integrated circuit, having all of the claimed features as discussed above with respect claim 1, wherein there is a value of said capacitance associated with metal layers (column 5, lines 1-8) adjacent to said inductor layer 32, Fig. 9,

except, Forber doesn't teach a value of said negative capacitance is approximately equal in magnitude to said capacitance associated with metal layers adjacent to said inductor layer.

Gagne discloses in Fig. 3 a value of said negative capacitance is approximately equal in magnitude to said capacitance associated with metal layers adjacent to said inductor layer (column 3, lines 25-50). Therefore, at time the invention was made, it was well know to use a value of said negative capacitance is approximately equal in magnitude to said capacitance associated with metal layers adjacent to said inductor layer,

Therefore it would have been obvious to one of ordinary skill in the art, at time the invention was made for Forber to include in his invention a value of said negative capacitance is approximately equal in magnitude to said capacitance associated with metal layers adjacent to said inductor layer,

Benefit of doing so is to provide inductor with high quality factor.

3.1.3. Regarding claim 3: Forber discloses the integrated circuit, having all of the claimed features as discussed above with respect claim 1,

except, Forber doesn't teach said circuitry comprises: at least two transistors; at least two resistors; each resistor of said at least two resistors being coupled to each of said at least two transistors; a capacitor coupled to a first transistor of said at least two transistors and a first resistor of said at least two resistors.

Gagne discloses in Fig. 3a said circuitry comprises: at least two transistors A1 and A3; at least two resistors R_1 and Rm1; each resistor of said at least two resistors being coupled to each

of said at least two transistors; a capacitor C_1 coupled to a first transistor of said at least two transistors and a first resistor R_1 of said at least two resistors. Therefore, at time the invention was made, it was well know to use said circuitry comprises: at least two transistors; at least two resistors; each resistor of said at least two resistors being coupled to each of said at least two transistors; a capacitor coupled to a first transistor of said at least two transistors and a first resistor of said at least two resistors.

Therefore it would have been obvious to one of ordinary skill in the art, at time the invention was made for Forber to include in his invention said circuitry comprises: at least two transistors; at least two resistors; each resistor of said at least two resistors being coupled to each of said at least two transistors; a capacitor coupled to a first transistor of said at least two transistors and a first resistor of said at least two resistors.

Benefit of doing so is to provide circuit for compensation for a capacitance associated with metal layers.

3.1.4. Regarding claim 4: Further, Forber, as modified, discloses the integrated circuit, having all of the claimed features as discussed above with respect claim 3, wherein said at least two transistors are at least one of bipolar transistors, MOSFETS (column 4, lines 1-4), and gallium arsenide pseudomorphic high-electron mobility transistors.

3.1.5. Regarding claim 5: Further, Forber, as modified, discloses the integrated circuit, having all of the claimed features as discussed above with respect claim 3,

except, Forber doesn't teach said negative capacitance generated by said circuitry is dependent upon component values of said at least two resistors and said capacitor.

Gagne discloses in Fig. said negative capacitance generated by said circuitry is dependent upon component values of said at least two resistors R_1, R_2 and Rm1, and said capacitor C_1. Therefore, at time the invention was made, it was well know to use said negative capacitance generated by said circuitry is dependent upon component values of said at least two resistors and said capacitor.

Therefore it would have been obvious to one of ordinary skill in the art, at time the invention was made for Forber to include in his invention said negative capacitance generated

by said circuitry is dependent upon component values of said at least two resistors and said capacitor, motivated by its known suitability for its intended use. See MPEP §2144.07.

3.1.6. Regarding claim 6: Further, Forber, as modified, discloses the integrated circuit, having all of the claimed features as discussed above with respect claim 1, wherein said circuitry is fabricated within the substrate (Fig. 8 and column 3, lines 50-67).

4.1. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yuriy Semenenko whose telephone number is (571) 272-6106. The examiner can normally be reached on 8:30am - 5:00pm.

4.2. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on (571)- 272-1957. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

4.3. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

YS

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